**Shylaja Balagopal**

408-685-5453  shylajab@yahoo.com

**Digital Verification Engineer**

***Delivering top quality through expertise in verification***

Highly motivated ASIC Verification Engineer with a record of achievement in verifying design from concept to production on accelerated schedules. Proven ability to build testbenches, traffic generators, drivers, monitors and scoreboard, and test plan/test cases in SystemVerilog, C++, C, and Assembly language and testbenches in Verilog HDL and Vera. Skilled in verifying systems on chips (SoCs) and creating test plans and test cases at both module and chip levels. Exceptional debugging and Perl scripting skills. Areas of expertise include:

ASIC Design | Verification Flows | RTL Design | Simulation | Testbench Development | HVL | HDL  
SystemVerilog | Verilog | HVL Methodology (OVM/VMM) | Problem Solving  
Constrained Random Testing | Debugging | Scripts | Coverage Models | Silicon validation | Gate level simulation

**Technical Background**

SystemVerilog Testbenches, UVM, Verification Methodology Manual (VMM), Open Verification Methodology (OVM), Object-Oriented Programming (OOP), Verilog, Vera, Verplex, C, C++, Perl

**Professional Experience**

**NGC** **July 2023 – Present**

**VERIFICATION ENGINEER - Contract**

Creating testplan, verification environments to verify designs using UVM. Implementation, Integration and testing of RAL for communication designs.

**MICROSOFT** **July 2019 –May 2023**

**SENIOR STAFF VERIFICATION ENGINEER**

Worked on verification of XBOX products, L3 verification of AI chip and security products. Worked on creating testcases, debugging, coverage, regression and integrating changes in existing verification infrastructure in UVM. Worked in the lab on bring up, validation and debugging on silicon.

**INTEL** **Nov. 2016 – June 2019**

**ASIC STAFF VERIFICATION ENGINEER**

Working in an IP group for verification of DDR4 and LPDDR4. Working on coverage, debugging and writing testcases in UVM. Installing and integrating tools for register testing, regression and debug.

**Synaptics** **2014- Aug. 2016**

**ASIC STAFF VERIFICATION ENGINEER**

Convert and debug inter-integrated circuit (I2C) tests for a display project. Execute regressions and debugging at the system level. Develop test plan, test cases, and scripts, and debug modules for a smart pen project. Perform system-level testbench modifications. Contribute to analog/digital converter (ADC) debugging. Work on a fingerprint project to build, verify, and debug tests.

*Achievements*

* **Rapidly brought blocks up for the smart pen project, debugged, and verified** by collaborating with architects and multiple designers on different blocks simultaneously.
* **Shared knowledge and skills with the verification group** by delivering presentations on the formal verification process.

**ASIC Verification** **2011-2013**

**ENGINEER XILINX**

Conducted verification of digital signal processors (DSPs) utilizing assertion-based verification (ABV). Led engineers to verify block RAM (BRAM) and DSP using OVM. Developed test plans, ran regression, debugged, and managed schedules.

*Achievements*

* **Ensured the delivery of tapeout on schedule** by stepping up to help in completing verification of a senior engineer’s blocks after that team member’s departure from the company.

**Shyla LLC** **2009-2011**

**ENGINEER CONTRACTOR**

Developed a SystemVerilog testbench, including drivers, monitors, and scoreboard for multiple field-programmable gate arrays (FPGAs). Performed ABV. Created test plans and test cases and conducted debugging. Contributed to bring up and debugging work for the FPGA in the lab. Debugged designs using ISE and Chipscope and a formal verification tool from Cadence ABV.

*Achievements*

* **Delivered significant contributions on accelerated schedules** for multiple designs.
* **Recognized for collaborating effectively with designers** in creating the test plan, identifying bugs in designs, offering solutions for the bugs, and debugging the FPGA in the lab using Chipscope and ISE.

**Cisco** **2007-2008**

**ASIC DESIGN VERIFICATION ENGINEER**

Built a constrained random SystemVerilog testbench, including traffic generators, drivers, monitors, and scoreboard for the packet distribution module as part of a high-end network processor project. Based the environment on the VMM with heavy use of OOP. Developed test cases in aspect-oriented programming (AOP) to further constrain the environment. Authored the test plan and environment specifications. Devised the design verification (DV) environment to test rate limiter as part of the design reuse module. Wrote code to create a DV reuse component for the rate monitor. Created a testbench, driver, monitor, and test cases for the link scheduler.

*Achievements*

* **Delivered bug-free blocks to production** via effective verification; transmitted design to production with no bug subsequently found since verification in 2008.

**McData Corp** **2005-2007**

**SR. ASIC VERIFICATION ENGINEER**

Provided conversion from C++ to Vera and integration for the behavioral model of the packet processor. Authored the test plan and test cases and debugged features, including Inter-fabric routing.

*Achievements*

* **Served in a highly critical role** after multiple several senior engineers left for start-ups, successfully completing the task of verifying the packet processor and finding multiple critical bugs in the process.
* **Secured quality** by identifying a corner case bug that would have caused respin.

**Education**

**Master of Science in Computer Engineering**

**The University of Texas at Austin**

*Thesis:* *Implementation of Sampling Techniques for Design Error Simulation Coverage:* By implementing sampling techniques, the thesis provides a means of design verification of large VLSI circuits for a simulation automation system developed at the University of Texas at Austin.

**Bachelor of Science in Electrical and Electronics**

**Annamalai University, Chidambaram, India**